ITC576A 1200 dpi CIS Wafer

Preliminary Data

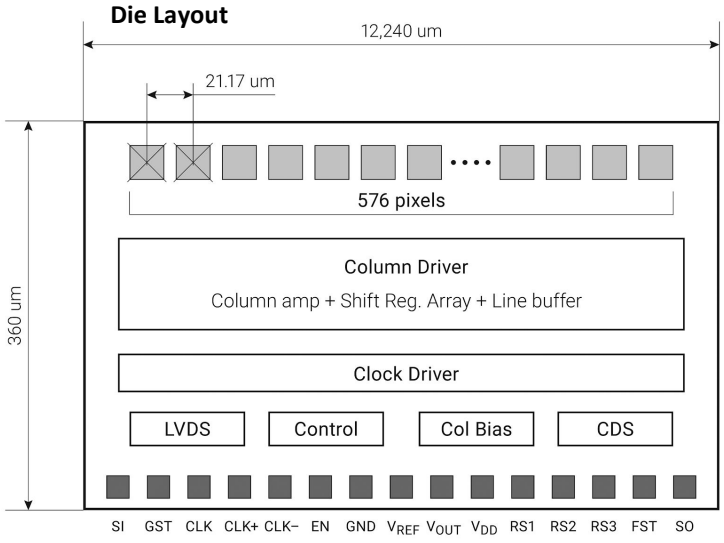
Description

ITC576A is a high performance linear Contact Image Sensor (CIS). It supports a wide range of resolutions - 1200, 600, 400, 300, 200, 100 dots per inch (dpi) - and operates at up to 40 MHz. A Low Voltage Differential Signaling (LVDS) clock interface enables high speed operation and wider module assemblies with lower noise. The ITC576A includes an output amplifier, which provides sample & hold video output that implements Correlated Double Sampling (CDS). The Sensor includes a global shutter mechanism in which the values read out during the present line time are the values that were integrated in the photodiodes during the previous line readout period.

Features

- Chip resolution: 1200/600/400/300/200/100 dpi
- Single power supply: 3.3V
- # of Pixels: 576@1200dpi
- Pixel to pixel spacing: 21.1666@1200dpi, 63.5um@400 dpi
- Pixel data rate: 40 MHz Max.
- LVDS differential clock interface, CMOS compatible
- LVDS driver included in each die
- Sensor response non-uniformity: ± 10%
- Chip sensitivity: High Gain 2400 V/uJ/cm² (wavelength)
- Random noise: 4 mV (typical)
- Saturation Voltage: Max 1.5V (from dark level)
- Pixel level CDS to reduce pixel FPN and reset noise
- Line buffer/storage to allow data read during integration
- On chip timing, amplifier and control
- Control logic enables “daisy-chaining” of multiple dies
- Chip size(L x W): 12,240 µm × 360 µm
- Operating temperature: -10 ~ 50
- Available as 200 mm wafer - back thinned to 250 µm

Die Layout

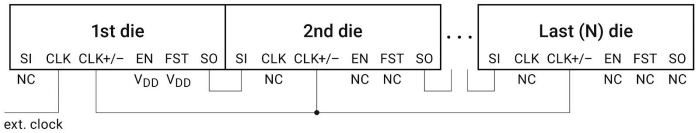


Timing Summary

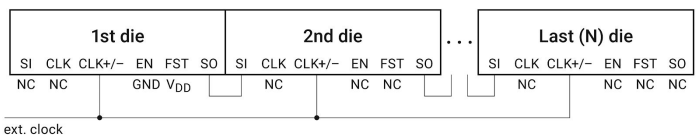
Item	Symbol	Min	Typ	Max	Unit	Note
Clock frequency	f	1		40	MHz	
CLK period	t_{CLK}	25		1000	ns	1 ~ 40MHz
CLK pulse duty[1]	DC	45	50	55	%	Duty cycle
CLK rise/fall time	t_1		1.0		ns	
GST period	t_{GST}		1 CLK			25ns @ 40Mhz
GST setup time	t_S	2			ns	
GST hold time	t_H	2			ns	
GST rise/fall time	t_2		1.0		ns	
SO rise/fall time	t_3		1.0		ns	
Vout delay time[2]	t_{VD}	5ns		6.5ns		
Vout latency			35		clocks	On first die

[1] Defined as the ratio of the positive duration of the clock to its period
[2] CLK to internal clock delay is 2ns, Vout amplifier delay time is approx. 3ns. Responsive to falling edge of clock. ADC should be triggered on rising edge to capture middle of pixel output.

Typical Application



< LVDS clock configuration using internal driver on die #1 >



< LVDS clock configuration with external LVDS >

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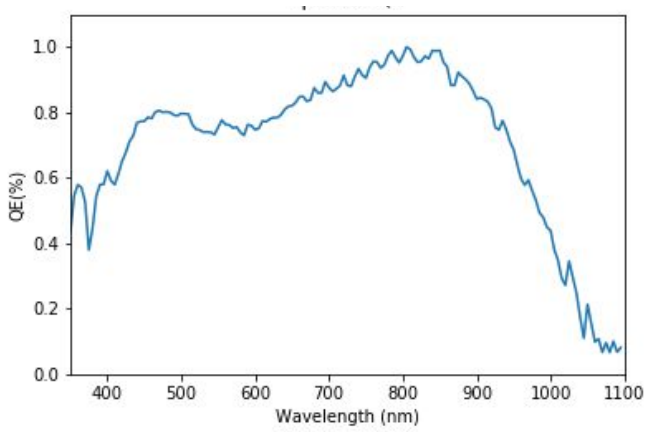
Normalized Quantum Efficiency



Complete electro-optical performance data will be available upon completion of first lot evaluation.

Wafer Configuration

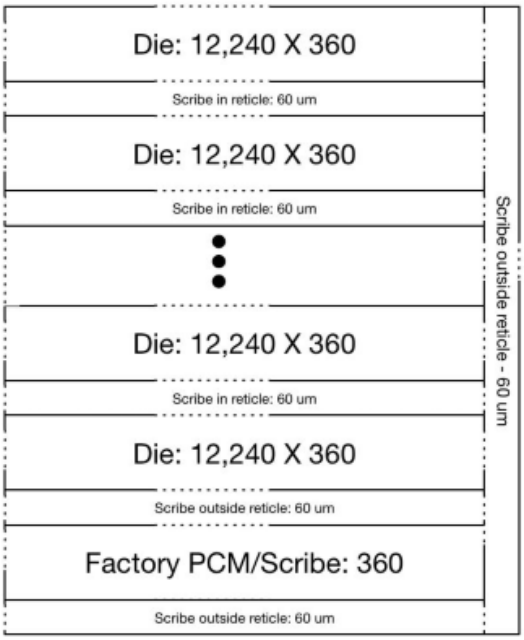
- 200 mm (8-inch) diameter with notch
- 254 µm thickness, background

Pad Functions and Locations

Pin#	Name	Type	Note	Pad position (center of Pad)
1	SI	CMOS INPUT	Scan In / Start of Scan, active High - Internal Pulldown (can be NC when not used)	(2213.5,78.5) um
2	GST	CMOS INPUT	Global Start pulse, active High - Internal Pulldown (can be NC when not used)	(2813.5,78.5) um
3	CLK	CMOS INPUT	External Clock (active when EN active) - Internal Pull-down (can be NC when not used)	(3413.5,78.5) um
4	CLK+	LVDS I/O	LVDS differential clock, positive signal - Output when EN high or NC - Input when EN low	(4013.5,78.5) um
5	CLK−	LVDS I/O	LVDS differential clock, negative signal - Output when EN high or NC - Input when EN low	(4613.5,78.5) um
6	EN	CMOS INPUT	Clock Enable set (VDD: LVDS TX enabled, GND or NC: LVDS TX disabled) - Internal Pull-down (can be NC to disable)	(5213.5,78.5) um
7	GND	Power	Ground	(5813.5,78.5) um
8	VREF	Analog Input	Reference voltage	(6413.5,78.5) um
9	VOUT	Analog Output	Video out positive, sample & hold c/w CDS	(7013.5,78.5) um
10	VDD	Power	3.3V	(7613.5,78.5) um
11	RS1	CMOS INPUT	DPI selection 1 - Internal Pullup	(8213.5,78.5) um
12	RS2	CMOS INPUT	DPI selection 2 - Internal Pulldown	(8813.5,78.5) um
13	RS3	CMOS INPUT	DPI selection 3 - Internal Pullup	(9413.5,78.5) um
14	FST	CMOS INPUT	1st die Enable (VDD: 1st die, GND or NC: other dies) - Internal Pull-down (can be NC to disable)	(10013.5,78.5) um
15	SO	CMOS OUTPUT	Scan Out / End of scan, active High	(10613.5,78.5) um

Pad size is 95 x 95 µm.

Wafer Shot Map



No performance guarantees are made by this document. All specifications are subject to change without notice at the sole discretion of the manufacturer.

Full specifications available upon execution of a Non-Disclosure Agreement

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